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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,173	07/21/2003	Michael John Erickson	10981624-2	2724

22879 7590 03/09/2005

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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,173	ERICKSON ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-23* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on December 3, 2004

2. This application has been examined. Claims 1-23 are pending.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 14-15, 17-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Busby (US No. 4,245,270).

In regard to claim 1, Busby discloses an apparatus for indicating the insertion and removal of a circuit board for hot swap applications comprising: a logic circuit (G1, G2) having at least one input (21, 26, 24, 25) and at least one output (31) (see figure 1, col. 2, line 60 through col. 3, line 14); and a time extender circuit (i.e. RC circuit) (R3, C2) connected to said logic circuit, for extending an output signal of said logic circuit for a period of time after said circuit board is completely inserted and removed (see figure 1, col. 3, lines 26-65).

In regard to claim 2, Busby discloses wherein said logic circuit further comprises a NAND gate (see col. 2, lines 60-65).

In regard to claim 3, Busby discloses wherein said NAND gate further comprises: a plurality of transistors connected in parallel having a plurality of inputs and at least one output (see figure 1, col. 2, lines 60-67).

In regard to claim 4, Busby further discloses an enable logic gate (G3) connected to said at least one output of said logic circuit (see figure 1, col. 3, lines 1-7).

In regard to claim 5, Busby further discloses a transistor configured as an open collector having an input and an output whose input is connected to said at least one output of said logic circuit (see col. 2, line 60 through col. 3, line 14).
In regard to claim 6, Busby discloses wherein said time extender circuit further comprises: a resistor connected between ground and said logic circuit; and a capacitor connected between a voltage and said logic circuit (see col. 3, line 26 through col. 4, line 22).

In regard to claim 14, Busby discloses a method for indicating the insertion and removal of a circuit board, comprising: receiving at least one input signal indicating the insertion and removal of a circuit board (see col. 4, lines 22-64); processing said at least one input signal indicating the insertion and removal of a circuit board (see col. 4, lines 22-64); generating an output signal indicating said insertion and said removal of said circuit board (see col. 4, lines 22-64); and extending said output signal for a period of time after said circuit board is completely inserted and removed (see col. 4, line 29 through col. 5, line 41).

In regard to claim 15, Busby further discloses the step of enabling said output signal (i.e. output signal from G3) (see figure 1, col. 4, lines 3-64).

In regard to claim 17, Busby discloses wherein said step of extending said output signal for a period of time after said circuit board is completely inserted or extracted further comprises the step of discharging a capacitor (see col. 5, lines 31-41).

In regard to claims 18, 21, Busby further comprising the steps of: outputting a plurality of complementary control signals (see col. 4, lines 3-64); performing a logic operation using one of said complementary control signals and said output signal to produce a logic output (see col. 4, lines 3-64); using said logic output from said logic operation to source current (see col. 4, lines 3-64); and sinking current using said input signal (see col. 3, lines 40-46).

In regard to claim 19, Busby discloses wherein said step of processing further comprises the step of performing a logic function on said at least one input signal (see col. 4, lines 3-64).

In regard to claim 20, Busby discloses wherein said logic function further comprises the step of performing a NAND logic function on said at least one input signal (see col. 4, lines 3-64).

In regard to claim 22, Busby discloses wherein said step of sinking current further comprises using another of said plurality of complementary control signals to sink said current to ground or through a resistor to ground (see col. 5, lines 42-59).

In regard to claim 23, Busby discloses wherein said step of outputting a plurality of complementary control signals further comprises applying a threshold voltage (see col. 3, lines 9-40).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7-8, 11, 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Busby in view of Nakaoka (US No. 4,886,984).

In regard to claim 7, Busby discloses the claimed subject matter as discussed above rejection except the teaching of at least one inverter having an input and an output, wherein said input of said at least one inverter is connected to an output of said NAND gate. However Nakaoka discloses at least one inverter 48 having an input and an output, wherein said input of said at least one inverter is connected to an output of said NAND gate 47 (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

In regard to claim 8, Nakaoka further discloses at least one inverter having an input and an output, wherein said input of said at least one inverter is connected to said at least one output of said plurality of transistors (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

In regard to claim 11, Nakaoka further discloses an enable logic gate connected to at least one of said outputs of said at least one inverter; and a transistor configured as an open collector having an input and an output whose input is connected to at least one of said outputs of said at least one inverter (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

In regard to claim 16, Nakaoka further discloses the step of inverting said output signal (see figure 3, col. 6, lines 43-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Nakaoka within the system of Busby because it would provide a prohibition circuit upon power on event which prohibits power consuming circuits from undesirable operation after the power switch on event.

8. Claims 9-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Busby in view of Nakaoka and further in view of Dorsey et al. (US No. 5,910,690).

In regard to claims 9-10, even though the teachings of Nakaoka or Busby does not disclose the inverter is a Schmitt trigger inverter, however Dorsey et al. disclose the inverter circuit is a Schmitt trigger inverter (see figure 11, col. 12, lines 26-47). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dorsey et al. within the system of Nakaoka and Busby because it would provide

a desirable control to the switching mechanism during the insertion or removal of the cards.

9. Claims 12-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Busby in view of Dorsey et al.

In regard to claim 12, Busby discloses an apparatus for indicating the insertion and removal of a circuit board, comprising: a plurality of transistors (G1, G2) connected in parallel having at least two inputs (21, 26, 24, 25) and at least one output (31) (see figure 1, col. 2, line 60 through col. 3, line 24); at least one other transistor (G3) having at least one output and at least one input connected to said at least one output of said plurality of transistors connected in parallel (see figure 1, col. 2, line 60 through col. 3, line 24); a time extender circuit (i.e. RC circuit (R3, C2) connected to said at least one output of said at least one other transistor (see figure 1, col. 3, lines 26-65). But Busby does not specifically disclose at least one Schmitt trigger inverter having an input connected to said output of said at least one other transistor. However Dorsey et al. disclose at least one inverter 230 having an input and an output, wherein said input of said at least one inverter is connected to an output of said transistor (see figure 11, col. 12, lines 26-47). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Dorsey et al. within the system of Busby because it would provide a desirable control to the switching mechanism during the insertion or removal of the cards.

In regard to claim 13, Dorsey et al. further disclose a transistor configured as an open collector having an input and an output whose input is connected to said output of said at least one inverter (see figure 11, col. 12, lines 26-47). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the

invention was made to have combined the teachings of Dorsey et al. within the system of Busby because it would provide a desirable control to the switching mechanism during the insertion or removal of the cards.

Allowable Subject Matter

10. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. In view of remark filed on November 25, 1997, claims 5-10 have been fully considered but they are not deemed to be persuasive.

Applicant(s) argue that ...Busby. fails to teach the time extender circuit connected to the logic circuit, for extending an output signal of the logic circuit for a period of time after the circuit board is completely inserted and removed (see page 6). The Examiner does not agree. Busby teaches the RC circuit which ouputs the signals to the logic (i.e. transistor) for a period of time after the disconnecting of pin P3 (i.e. shortest pin connected to the voltage) and that's completely removed from the power (see col. 4, lines 35-49).

Conclusion

12. All claims are rejected. Claim 6 is objected.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE

CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (571) 272-3639 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to **[raymond.phan@uspto.gov]**.

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see hop://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

Raymond Phan
3/4/05